N-Channel 30V (D-S)MOSFET

GENERAL DESCRIPTION

The 3400A is the N-Channel logic enhancement mode power field effect transistors, using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone, notebook computer power management and other battery powered circuits, and low in-line power loss that are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 30m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leqq 35m\Omega @ V_{GS}=4.5V$
- $R_{DS(ON)} \leqq 52m\Omega @ V_{GS}=2.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

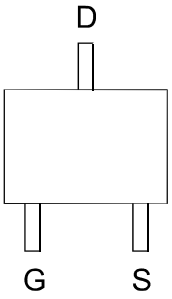
APPLICATIONS

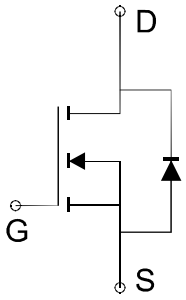
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION

(SOT23-3L)

Top View





Ordering Information: 3400A (Pb-free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current	T_A=25℃	I_D	5.8	A
	T_A=70℃		4.9	
Pulsed Drain Current		I_{DM}	21.5	
Maximum Power Dissipation	T_A=25℃	P_D	1.39	W
	T_A=70℃		0.89	
Operating Junction and Storage Temperature Range		TJ, Tstg	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	90	℃/W

*The device mounted on 1in2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC PARAMETERS						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	0.7		1.4	
I_{GSS}	Gate-Body Leakage Current	V_{DS}=0V, V_{GS}=±12V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance[a]	V_{GS}=10V, I_D= 5.8A		25	30	mΩ
		V_{GS}=4.5V, I_D= 3.5A		29	35	
		V_{GS}=2.5V, I_D= 2.8A		39	52	
V_{SD}	Diode Forward Voltage	I_S=1.25A, V_{GS}=0V		0.8	1.2	V
DYNAMIC PARAMETERS						
Qg	Total Gate Charge	V_{DS}=15V, V_{GS}=10V, I_D=4A		15.5		nC
Qgs	Gate-Source Charge			3.2		
Qgd	Gate-Drain Charge			3.5		
Rg	Gate Resistance	f =1MHz		0.7		Ω
Ciss	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHz		480		pF
Coss	Output Capacitance			70		
Crss	Reverse Transfer Capacitance			18		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=15V, R_L =15Ω I_D=1A, V_{GEN}=10V, R_G=6Ω		8.5		ns
t_r	Rise Time			17		
$t_{d(off)}$	Turn-Off Delay Time			31		
t_f	Fall Time			3		

Notes: pulse width ≦ 380us, duty cycle≦ 2%

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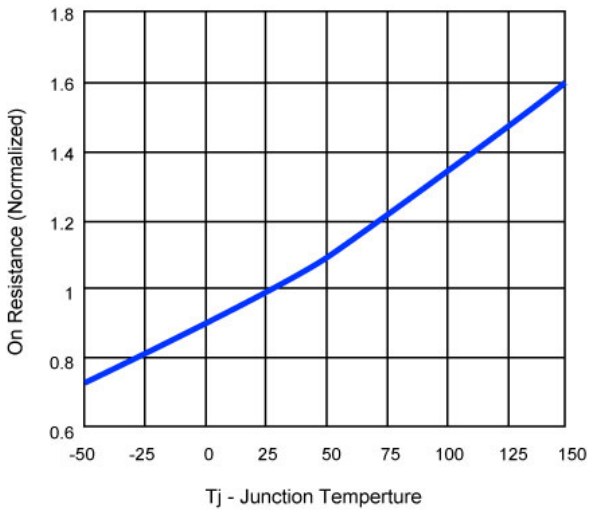
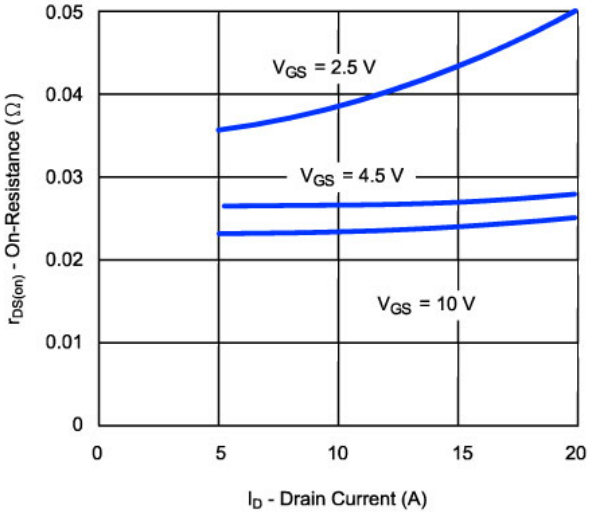
Typical Characteristics (T_J =25℃ Noted)

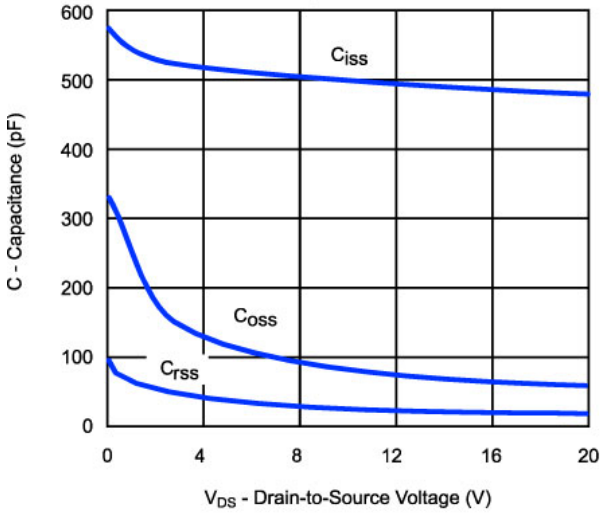
On Resistance vs. Junction Temperture



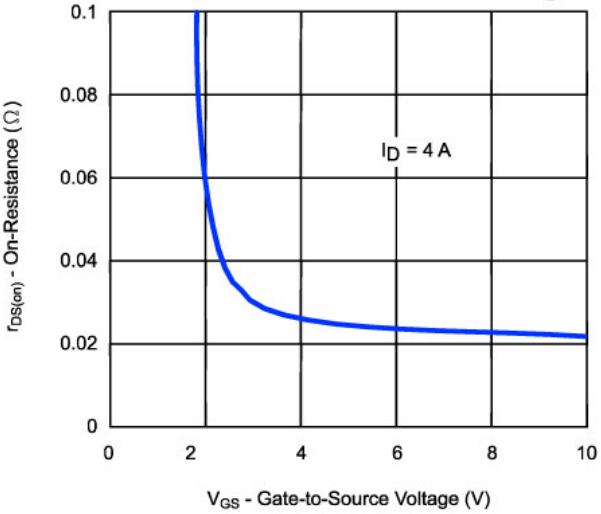
On-Resistance vs. Drain Current



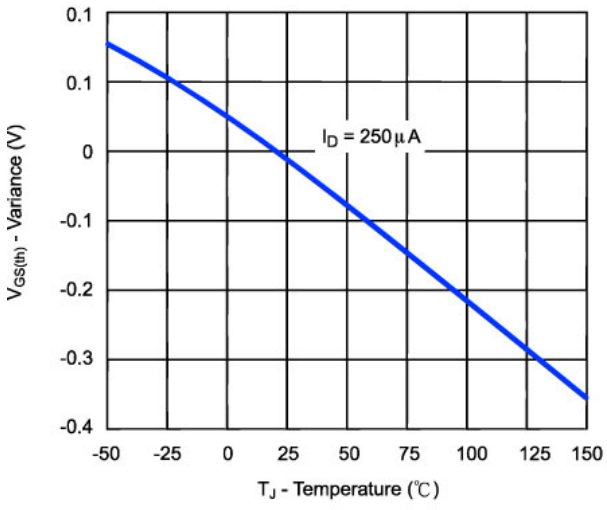
Capacitance



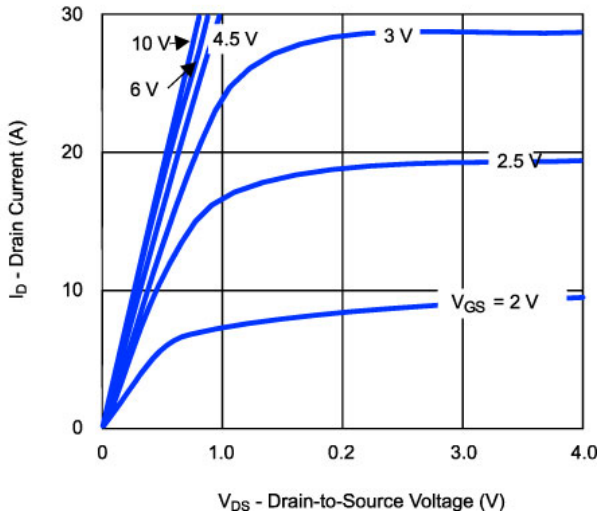
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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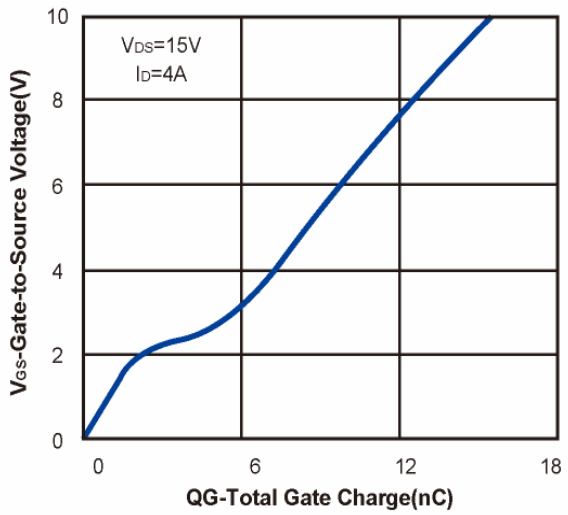
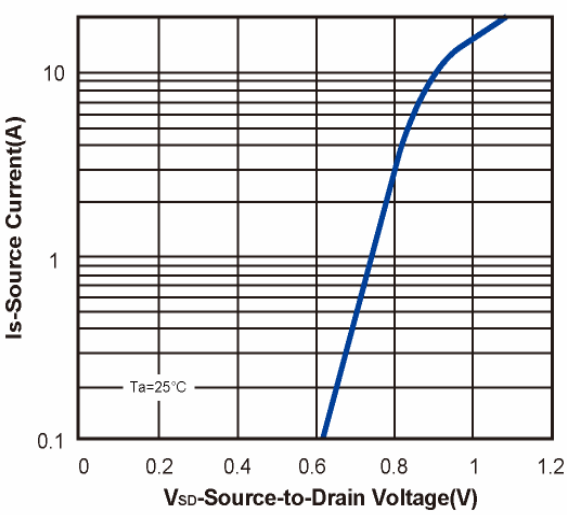
Typical Characteristics (T_J =25℃ Noted)

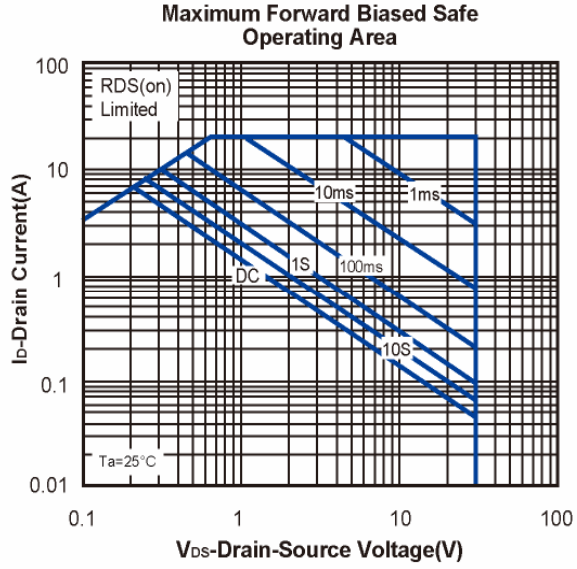
Gate Charge



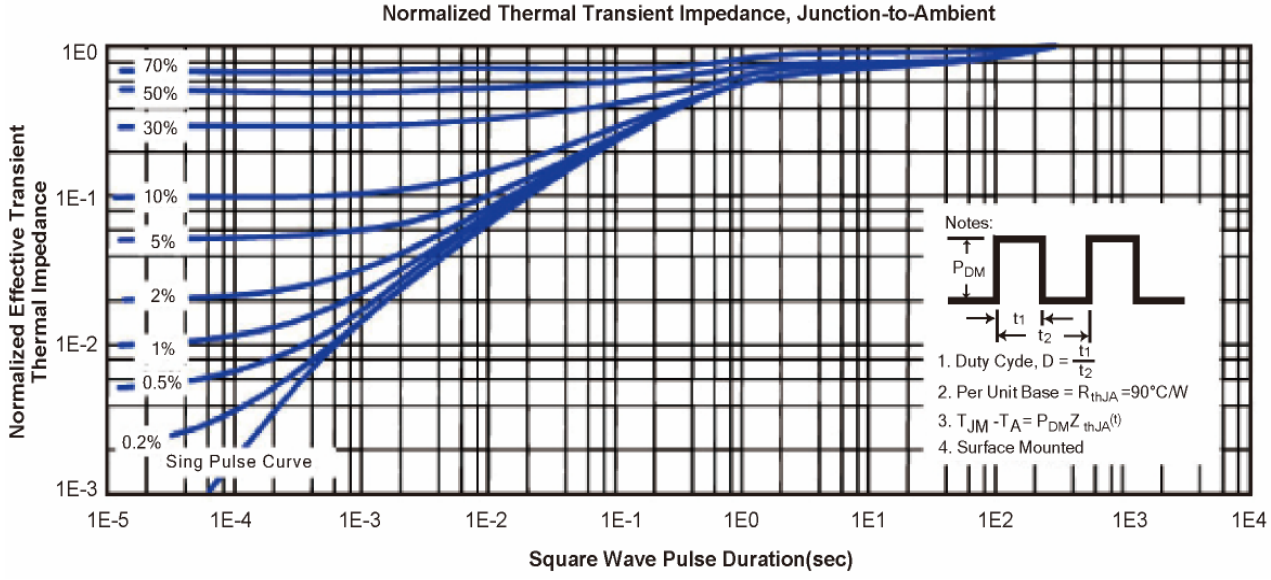
Body-diode characteristics



Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



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SOT23-3L Package Outline